

(51) International Patent Classification 6 :
G08B 13/14

A1

(11) International Publication Number: WO 00/16277
(43) International Publication Date: 23 March 2000 (23.03.00)

(21) International Application Number: PCT/US99/20307
(22) International Filing Date: 3 September 1999 (03.09.99)
(30) Priority Data: 09/151,568 11 September 1998 (11.09.98) US
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(81) Designated States: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, UZ, VN, YU, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BI, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published
With international search report.

(54) Title: METHOD AND APPARATUS FOR AN OPTIMIZED CIRCUIT FOR AN ELECTROSTATIC RADIO FREQUENCY IDENTIFICATION TAG

(57) Abstract

A radio frequency identification (RFID) tag (100), optimized for electrostatic applications, includes a first antenna element (112), second antenna element (114) and an RFID circuit (116). The first antenna element is electrically isolated from the second antenna element. The RFID circuit has a first pad (230) and a second pad (232) with an input capacitance between them. The first and second pads of the RFID circuit are coupled, respectively, to the first and second antenna elements. The RFID circuit includes a load modulation circuit (222) coupled to at least one of the first or second pads to produce a load modulated signal on at least one of the first or second pads that varies from a first amplitude to a second amplitude. The load modulation circuit has a modulation impedance and a predetermined voltage threshold that an input signal must exceed before the modulated signal is produced.

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5 METHOD AND APPARATUS FOR AN OPTIMIZED CIRCUIT
FOR AN ELECTROSTATIC RADIO FREQUENCY
IDENTIFICATION TAG

10 Field of the Invention

The invention relates generally to radio frequency identification tags, and in particular, to a circuit and method for optimizing electrostatic radio frequency identification tags.

15 Background of the Invention

Remotely powered electronic devices and related systems are known. For example, U.S. Patent No. 5,009,227 issued to Geiszler et al. entitled Proximity Detecting Apparatus, discloses a remotely powered device which uses electromagnetic coupling to derive power from a remote source and
20 then uses both electromagnetic and electrostatic coupling to transmit stored data to a receiver often collocated with the remote source. Such remotely powered communication devices are commonly known as radio frequency identification ("RFID") tags.

Radio frequency identification tags and associated systems have numerous uses. For example, radio frequency identification tags are frequently used for personal identification in automated gate sentry applications protecting secured buildings or areas. These tags often take the form of access control cards. Information stored on the radio frequency identification tag identifies the person seeking access to the secured building
30 or area. Older automated gate sentry applications require the person accessing the building to insert or swipe their identification tag or card into or through a reader for the system to read the information from the identification tag. Newer radio frequency identification tag systems allow the radio frequency identification tag to be read at a small distance using radio frequency data transmission technology, thereby eliminating the need to
35 insert or swipe an identification tag into or through a reader. Most typically, the user simply holds or places the radio frequency identification tag near a

base station, which is coupled to a security system securing the building or area. The base station transmits an excitation signal to the radio frequency identification tag that powers circuitry contained on the radio frequency identification tag. The circuitry, in response to the excitation signal, communicates stored information from the radio frequency tag to the base station, which receives and decodes the information. The information read is used by the security system to determine if access is appropriate. Also, radio frequency identification tags are written remotely by an excitation signal appropriately modulated in a predetermined manner.

In addition to typical applications for access control of persons, RFID tags are useful in applications identifying things, such as electronic animal identification, baggage tracking, parcel tracking, inventory management applications, asset identification and tracking, and other applications. These applications involve transmitting stored information from a tag to an exciter/reader system in close proximity with the tag. These applications may also involve transmitting information from the exciter to the tag for storage on the tag.

Earlier RFID tags and systems primarily use electromagnetic coupling to remotely power the remote device and couple the remote device with an exciter system and a receiver system. The exciter generates an electromagnetic excitation signal to power up the device and the receiver receives the signal produced by the remote device.

Earlier electromagnetic coupling mechanisms include an oscillator as part of the exciter circuitry and a coil antenna on both the exciter circuitry and the remote tag that includes an electronic circuit. For example, in an earlier system, excitation circuitry is connected to a coil antenna, which radiates excitation signals that are picked up by a coil antenna mounted on a tag that also contains the electronic circuit. The excitation signals energize the circuit, which then provides an information-carrying signal that is transmitted to the receiver using electromagnetic or electrostatic coupling.

One problem with the use of electromagnetic coupling between a remote device and either an exciter or a receiver has been the complexity involved in the manufacture of remote devices that employ a coil antenna. The spiral layout of a typical coil antenna makes it more difficult to produce, increases cost and also the size of the remote device. Also, the coil antennas require tight tolerances for efficient performance.

Electrostatic coupling for RFID tags has been proposed to address the problems and cost associated with electromagnetic coupling. For electrostatically coupled RFID tags, the antenna coil or antenna coil and capacitor external to the electronic circuit are eliminated and replaced with cheaper electrostatic antennas which may be as simple as conductive ink printed on paper. The virtues of electrostatically coupled RFID tags are discussed in commonly assigned U.S. patent application serial number 08/540,813, filed 11 October, 1995 by Ted Geiszler et al., attorney docket number IND00701, entitled "Remotely Powered Electronic Tag and Associated Exciter/Reader and Related Method"; U.S. patent application serial number 09/031,848 filed 27 February 1998 by Victor Allen Vega et al., attorney docket number IND10153, entitled "Radio Frequency Identification Tag System Using Tags Arranged For Coupling to Ground"; U.S. patent application serial number 09/041,480, filed 12 March 1998 by Victor Allen Vega et al., attorney docket number IND10146, entitled "Radio Frequency Identification Tag Arranged For Magnetically Storing Tag State Information"; and U.S. patent application serial number 09/045,357, filed 20 March 1998 by Victor Allen Vega et al., attorney docket number IND10174, entitled "Radio Frequency Identification Tag With a Programmable Circuit State."

Electrostatic RFID tags typically use the same functional circuit blocks that are adapted for use with electromagnetic RFID tags. However, the characteristics of electrostatic coupling require different circuit considerations from electromagnetic coupling. One characteristic of electrostatic coupling that is different from electromagnetic coupling is the nature of the electrostatic and electromagnetic fields, and in particular, the roll-off in coupling voltage associated with the fields. This characteristic affects read ranges. Also, the impedance characteristics for electrostatic coupling are different from the impedance characteristics for electromagnetic coupling. Although some circuits for electromagnetic coupling have proved somewhat suitable for electrostatic coupling, circuit techniques exploiting the unique characteristics of electrostatic coupling have not been employed.

Therefore, there is a need for electronic circuits and methods of creating the same, which are optimized for the characteristics of electrostatic coupling of RFID tags.

Brief Description of the Drawings

FIG. 1 is a back plan view of a radio frequency identification tag in accordance with a preferred embodiment of the present invention.

FIG. 2 is a cross-sectional view of the tag of FIG. 1 taken along line 2-2.

5 FIG. 3 is a block diagram of a radio frequency identification tag system in accordance with a preferred embodiment of the present invention. —

FIG. 4 is a block diagram of another radio frequency identification tag system in accordance with a preferred embodiment of the present invention.

10 FIG. 5 is a schematic of a load modulation circuit of a radio frequency identification tag in accordance with a preferred embodiment of the present invention.

FIG. 6 is a schematic of an alternate load modulation circuit of a radio frequency identification tag in accordance with a preferred embodiment of the present invention.

15 FIG. 7 is a diagram illustrating an example load modulated signal from a load modulation circuit in accordance with a preferred embodiment of the present invention.

20 FIGS. 8A-D are embodiments of modulation impedance circuits for a load modulated circuit in accordance with a preferred embodiment of the present invention.

FIGS. 9A-D are embodiments of modulation switches for a load modulated circuit in accordance with a preferred embodiment of the present invention.

25 FIG. 10 is a schematic of an alternate load modulation circuit in accordance with a preferred embodiment of the present invention wherein the load modulation circuit includes a modulation threshold voltage.

FIGS. 11A-C are embodiments of threshold voltage circuits for a load modulated circuit in accordance with a preferred embodiment of the present invention.

30 FIG. 12 is a schematic of another alternate load modulation circuit in accordance with a preferred embodiment of the present invention wherein the load modulation circuit includes a modulation threshold voltage.

35 FIG. 13 is a schematic of another alternate load modulation circuit in accordance with a preferred embodiment of the present invention wherein the load modulation circuit includes a modulation switch incorporating a modulation threshold voltage.

FIG. 14 is a plan view of a die for a radio frequency identification circuit in accordance with a preferred embodiment of the present invention.

FIG. 15 is a schematic of a charge pump circuit in accordance with a preferred embodiment of the present invention.

5 FIG. 16 is a block diagram of a circuit eliminating the need for a charge pump in a radio frequency identification tag circuit in accordance with a preferred embodiment of the present invention.

FIG. 17 is a schematic of an embodiment of the circuit of FIG. 16.

10 FIG. 18 is a schematic of an embodiment of a radio frequency identification tag circuit in accordance with a preferred embodiment of the present invention wherein the load modulation circuit includes a circuit to selectively defeat load modulation.

15 FIG. 19 is a schematic of an embodiment of a radio frequency identification tag circuit in accordance with a preferred embodiment of the present invention wherein the load modulation circuit includes a circuit for electronic article surveillance (EAS), which is selectively defeated.

20 FIG. 20 is a schematic of a radio frequency identification tag circuit in accordance with an alternate preferred embodiment of the present invention wherein a transmit modulation circuit includes a circuit to selectively defeat modulation.

Detailed Description of the Preferred Embodiments

Briefly, a radio frequency identification tag in accordance with the present invention includes a first antenna element, a second antenna element
25 and a radio frequency identification circuit. The first antenna element is electrically isolated from the second antenna element. The radio frequency identification circuit has a first pad and a second pad. The first and second pads of the radio frequency identification circuit are coupled, respectively, to the first and second antenna elements. The radio frequency identification
30 circuit includes a load modulation circuit coupled to at least one of the first or second pads to produce a load modulated signal that varies from a first amplitude to a second amplitude. The load modulation circuit has a modulation impedance and a predetermined voltage threshold that an input signal must exceed before the load modulated signal is produced. The first
35 and second pads of the integrated circuit have a non-zero capacitance, as measured between the pads, hereinafter referred to as an input capacitance. In a preferred embodiment, the modulation impedance, predetermined

threshold voltage of the modulation circuit and the input capacitance are optimized for electrostatic operation. Also, in one embodiment, the integrated circuit has a charge pump for providing a high programming voltage to a memory. The integrated circuit is optimized to reduce the stages in the charge pump or alternatively, in another embodiment, to eliminate the need for the charge pump.

A method in accordance with the present invention includes the steps of: a) providing a first antenna element; b) providing a second antenna element electrically isolated from the first antenna element; c) providing a radio frequency identification circuit having a first pad and second pad and a load modulation circuit that produces a modulated signal that varies from a first amplitude to a second amplitude based on a modulation impedance; and d) coupling the first and second antenna elements to the first and second pads, respectively, of the integrated circuit. The integrated circuit has a modulation impedance, threshold voltage and input capacitance, all of which are optimized for electrostatic operation.

FIG. 1 shows one an embodiment of a radio frequency identification tag 100 in accordance with the present invention. Tag 100 has a substrate 110, a first antenna element 112, a second antenna element 114, and an integrated circuit 116. Substrate 110 provides a base for holding the components of tag 100. Formed on a back surface 109 of substrate 110 are first antenna element 112 and second antenna element 114. The first and second antenna elements 112, 114 are electrically isolated from each other. Integrated circuit 116 contains the electronics associated with tag 100 and is coupled to first antenna element 112 and second antenna element 114 via pads (not shown) on integrated circuit 116. Integrated circuit 116 is optimized for operation with tag 100 in accordance with the invention, as discussed below. Preferably, the front surface (not shown) of substrate 110 has indicia, which includes printed text, photographs, graphics or any other indicia.

FIG. 2 is a cross-sectional view of tag 100 taken along line 2-2 of FIG. 1. As best seen in FIG. 2, first and second antenna elements 112, 114 are disposed on substrate member 110. Integrated circuit 116 is coupled to first antenna element 112 and second antenna element 114.

Substrate 110 provides the base for tag 100. Substrate 110 is composed of any non-conductive component. Suitable materials for substrate 110 include paper, acetate, polyester, polyethylene, polypropylene, polypropylene with calcium carbonate, polyvinyl chloride, or plastic. The

selection of material for substrate 110 varies depending upon the application. For example, for an application wherein tag 100 is disposable, substrate 110 is preferably paper. For an application where tag 100 is durable and reusable, for example as an access control card, substrate 110 is preferably plastic, polyvinyl chloride or polyester.

First and second antenna elements 112, 114 are formed from numerous suitable conductive materials. The conductivity of antenna elements 112, 114 varies considerably with little or no performance degradation. For example, antenna elements 112, 114 with a resistivity from 0 ohms per square to 500 kilo ohms per square are operable for read-only applications. Antenna elements 112, 114 have a lower resistivity for write applications requiring higher programming current requirements. Suitable materials for antenna elements 112, 114 include conductive ink, wire, or a conductive metal material. More specifically, suitable materials for antenna elements 112, 114 include copper, graphite, metalized polyester, aluminum, silver ink and carbon ink. Antenna elements 112, 114 are placed on substrate 110 using any suitable process including printing, lamination, adhesively securing, and deposition. The shape of antenna elements 112, 114 is not limited, but preferably, for optimal performance, antenna elements 112, 114 consume substantially all of the available surface area on substrate 110. The impedance characteristics of antenna elements 112, 114 are preferably varied by the type of materials selected and by the dimensions and concentrations of the selected materials. For example, where conductive ink is used for antenna elements 112, 114, the deposition thickness of the conductive ink is used to vary the impedance characteristics. Unlike predecessor radio frequency identification tags that relied on electromagnetic coupling, antenna elements 112, 114 are not a coil.

Integrated circuit 116 houses the circuitry for powering up the radio frequency identification tag and sending a stored signal or information in response to receipt of an electrostatic exciter signal. For some applications, integrated circuit 116 includes the circuitry to write new information into the tag in response to an electrostatic exciter signal. The functions of integrated circuit 116 are discussed further below.

Integrated circuit 116 is coupled to first antenna element 112 and second antenna element 114 by any suitable manner that allows an electrical connection between the integrated circuit 116 and the antennas 112, 114, yet isolates antennas 112, 114 from each other. A preferred method for coupling

integrated circuit 116 to antennas 112, 114 is a conductive anisotropic adhesive that conducts in the "Z" direction, as shown in FIG. 2. Alternatively, an isotropic adhesive (conductive in all directions) is used as long as the isotropic adhesive used to couple first antenna 112 is isolated from the isotropic adhesive used to couple the second antenna 114 to the integrated circuit 116. An alternate method for coupling integrated circuit 116 to antennas 112, 114 is with double-sided, conductive, pressure sensitive adhesive tape. A preferred anisotropic adhesive tape is model number 9703 sold by 3M Corporation of Minneapolis, Minnesota. A preferred isotropic adhesive tape is model 335-1 sold by Ablestik of Rancho Dominguez, California. As another alternative, an anisotropic adhesive is applied over the entire, or selected portions of antenna elements 112, 114, or on the side of integrated circuit 116 that will be in contact with antenna elements 112, 114.

FIG. 3 is a block diagram illustrating a radio frequency identification tag system 200 including an exciter 202, reader 204 and tag 100. Exciter 202 is coupled to a first electrostatic antenna element 206 and a second electrostatic antenna element 208. Reader 204 is coupled to an antenna element 210. Integrated circuit 116 is electrically connected to first electrostatic antenna element 112 and second electrostatic antenna element 114 via pads 230 and 232, respectively, to form tag 100. Exciter 202 generates a signal that is electrostatically coupled to integrated circuit 116 from electrostatic antenna elements 206, 208 to electrostatic antenna elements 112, 114. The signal generated by exciter 202 may include information that is to be written to integrated circuit 116. In response to the signal from exciter 202, circuit 116 converts and regulates the coupled voltage, writes the appropriate information and generates a read signal that is electrostatically coupled over the air to reader 204 via electrostatic antenna element 210. Reader 204 reads the signal to decode the information for use by other systems (not shown).

Integrated circuit 116 includes a rectifier 214, a voltage regulator 215, a write decoder 216, a clock extraction circuit 217, a controller 218, a memory 220, a modulation encoder 221, a load modulator 222 and a charge pump 223. Rectifier 214 is coupled to antenna elements 112, 114 via pads 230, 232 to receive the electrostatically coupled signal from exciter 202. This alternating current (A.C.) signal is rectified by rectifier 214 to produce a direct current (D.C.) signal that is then regulated by voltage regulator 215 to provide a power supply voltage V_{cc} for integrated circuit 116. The A.C. signal from

exciter 202 is received by clock extraction circuit 217, which extracts a clock signal CLK that is used for clocking the components on integrated circuit 116. The A.C. signal from exciter 202 is passed to write decoder 216. Write decoder 216 decodes the information modulated into the signal by exciter 202 to determine the appropriate action to be taken by integrated circuit 116. More specifically, write decoder 216 is coupled to controller 218, which controls a memory 220, which is written in response to an appropriate signal from exciter 202 and/or read from in response to an appropriate signal from exciter 202. A write decoder is described in commonly assigned U.S. patent application serial number 09/151,418, filed 9/11/98 by Victor Allen Vega, attorney docket number IND10185, entitled "A Contactless Capacitive Data Transmission System and Method." Information read from memory 220 is encoded into a modulated signal by modulation encoder 221. Modulation encoder 221 uses any suitable means of modulation to encode information read from memory 220, including phase modulation, amplitude modulation, frequency modulation, or a combination of these. More specifically, modulation encoder 221 uses amplitude shift keying (ASK), frequency shift keying (FSK), or phase shift keying (PSK). The modulated signal from modulation encoder 221 is received by load modulator 222 which provides a load modulated signal that is electrostatically coupled through at least one of antenna elements 112, 114 to be received by reader 204. Load modulator 222 and alternative embodiments for this function are discussed further below. Charge pump 223 generates a high voltage V_{pp} required by memory 220 for programming.

FIG. 4 is a block diagram illustrating an alternate radio frequency identification tag system 300 in accordance with the present invention. Radio frequency identification tag system 300 includes a slightly modified integrated circuit 116'. The system 300 is similar to the system 200 except that load modulator 222 of integrated circuit 116 is replaced by transmit modulator 222' and is not coupled to first and second electrostatic antenna elements 112, 114, but is coupled to a separate electrostatic antenna element 302 via a pad 303. This embodiment advantageously has a separate electrostatic antenna element 302 dedicated for data transmission. Transmit modulator 222' couples a modulated signal based on modulation encoder 221 to antenna element 302 via pad 303.

FIG. 5 is a schematic diagram of load modulator 222, in accordance with the present invention. Load modulator 222 is shown connected to pad

230, which is coupled to antenna element 112. Load modulator 222 includes a modulation impedance 400 and a modulation switch 402. Modulation impedance 400 is coupled in series to pad 230 and modulation switch 402. Modulation switch 402 is coupled in series with modulation impedance 400 and common. Modulation switch 402 receives an input signal I, which preferably is a modulated bit stream of information from modulation encoder—221 (FIG. 3). Input signal I is used to control the "on" and "off" operation of modulation switch 402.

Load modulator 222 drives pad 230 by reflective load modulation, which is also known as backscatter modulation, to produce an amplitude modulated signal, often referred to as a dampened or load modulated signal. In response to the differences in voltage levels for input signal I, for example, a logic "high" versus a logic "low," modulation switch 402 is turned "off" or "on." When modulation switch 402 is on, that is, a connection is made, pad 230 is loaded by modulation impedance 400. This varies the amplitude of any signal on pad 230. When modulation switch 402 is off, any signal on pad 230 is not so loaded.

FIG. 6 is a block diagram of an alternate load modulation circuit in accordance with the present invention, including load modulator 522. Load modulator 522 is similar to load modulator 222, except that load modulator 522 load modulates pad 230 and pad 232. Load modulator 522 consists of two load modulators 222, one connected to pad 230 and the other connected to pad 232. The modulation circuit shown in FIG. 6 is referred to as a symmetrical load modulation circuit in that signals on both pad 230 and pad 232 are load modulated in response to an input signal. The load modulation circuit shown in FIG. 5 is referred to as an asymmetrical load modulation circuit in that only a signal on one pad, pad 230, is load modulated.

Modulation impedance 400 is implemented in numerous ways. Example embodiments are shown in FIGS. 8A through 8D. FIG. 8A shows modulation impedance 400 implemented as a resistor. FIG. 8B shows modulation impedance 400 implemented as a capacitor. FIG. 8C shows modulation impedance 400 implemented as a series connected resistor and capacitor. FIG. 8D shows modulation impedance 400 implemented as a resistor and capacitor connected in parallel. Other embodiments are possible and known to those of skill in the art, including active devices, for example, field-effect transistors (FETs).

Modulation switch 402 is shown in FIGS. 5 and 6 as a switch, but is preferably implemented as a transistor. Numerous implementations for modulation switch 402 are known. Example embodiments are shown in FIGS. 9A through 9D. FIG. 9A shows modulation switch 402 implemented as an N-channel FET with the input signal I coupled to the gate. FIG. 9B shows modulation switch 402 implemented as a P-channel FET with the input signal I connected at the gate. FIG. 9C shows modulation switch 402 implemented as an NPN transistor with input signal I coupled to the base. FIG. 9D shows modulation switch 402 implemented as a PNP transistor with input signal I coupled to the base.

FIG. 7 shows an example of a loaded or dampened amplitude modulated signal produced by load modulator 222 or load modulator 522 at pad 230 or pad 232. As shown in FIG. 6, the modulated signal 600 has a first amplitude 601 and a second lower amplitude 604. The amplitude of modulated signal 600 is controlled by the load modulation circuit in response to the input signal I. The magnitude of the amplitude of modulated signal 600 is in part determined by the value of modulation impedance 400. In electromagnetic radio frequency identification tags, modulation impedance 400 has typically been made as low as approximately 100 ohms. However, for electrostatic radio frequency identification systems, the modulation impedance is chosen such that the modulation current is large enough for adequate operation. For electrostatic radio frequency identification tags, better performance and efficiency is achieved with a higher modulation impedance. Preferably, for electrostatic systems, the modulation impedance is at least 1 kilo ohm and, most preferably, in the range of 1.5 to 10 kilo ohms. The larger modulation impedance improves read ranges and also reduces the current consumption of the chip. Another advantage is reduced emissions.

Antenna elements 112 and 114, which are connected in series with pad 230 and pad 232, respectively, affect the total modulation impedance of the load modulation circuit. That is, the impedance of antenna elements 112, 114 is combined with the associated modulation impedance to create an effective modulation impedance. Also, the impedance of antenna elements 112, 114 may be considered as an input series resistance to protect integrated circuit 116 from electrostatic discharge damage. Preferably, integrated circuit 116 is designed to minimize the effects of the impedance of antenna elements 112, 114.

FIG. 10 shows an alternate load modulation circuit in accordance with the present invention, including load modulator 622. Load modulator 622 is shown connected in series with pad 230 and common. Load modulator 622 is similar to load modulator 222, except that a modulation threshold voltage is shown schematically in series with modulation switch 402 and common. Modulation threshold voltage 602 requires that the input signal I achieve a certain threshold voltage before modulation switch 402 is turned on to load or dampen a signal on pad 230. Indeed, modulation switch 402 typically, inherently has a threshold voltage that input signal I must exceed prior to a signal on pad 230 being dampened or load modulated. However, for certain applications, it is desirable to adjust the threshold voltage.

Modulation threshold voltage 602 is implemented in numerous ways. Example embodiments for modulation threshold voltage 602 are shown in FIGS. 11A through 11C. FIG. 11A shows modulation threshold voltage 602 implemented as a zener diode of a certain voltage. FIG. 11B shows modulation threshold voltage 602 implemented as an N-channel FET with the gate connected to the source. FIG. 11C shows modulation threshold voltage 602 implemented as two N-channel FETs in series, both having their gates connected to their respective sources. Modulation threshold voltage 602 is alternatively implemented in a number of other ways, including stacking additional FETs in series or using alternative circuit components. Modulation threshold voltage 602 is alternatively adjusted by semiconductor processing as is well known in the art. Also, modulation threshold voltage 602 is alternatively combined with modulation switch 402, as discussed further below with respect to FIG. 13.

FIG. 12 is a block diagram of a preferred alternate load modulator 722 in accordance with the present invention. Load modulator 722 is a symmetric load modulator. That is, load modulator 722 modulates signals on pad 230 and pad 232. Load modulator 722 includes two load modulators 622, one of which is connected to pad 230 and the other connected to pad 232.

FIG. 13 is a schematic diagram of another alternate embodiment of a load modulation circuit in accordance with the present invention, including load modulator 822. Load modulator 822 is symmetrical. Load modulator 822 includes modulation impedance 400 and modulation switch 802, which has an inherent threshold voltage. Modulation switch 802 includes two groups 804 of nested transistors. Each group 804 of nested transistors includes three nested transistors connected in a Darlington configuration with

the collectors tied in common and the emitter of one transistor connected to the base of the succeeding transistor. The number of transistors in the Darlington configuration is variable depending upon the desired threshold voltage. For the circuit shown in FIG. 13 with three nested transistors, the equivalent of three times the threshold voltage of each transistor is the required modulation threshold voltage.

The ability of the input signal I to achieve a certain threshold voltage is determined in part by the power supply voltage produced by rectifier 214. This power supply voltage is in turn a function of the alignment of the tag with the exciter/reader, the orientation of the tag with the exciter/reader and the distance between the tag and the exciter/reader. Hence, the distance between the tag and exciter affects the ability of the input signal to attain a threshold voltage to produce a modulated signal. For improved read ranges in electrostatic applications, it is desirable to reduce the threshold voltage required to generate a modulated signal to allow communication between the tag and a exciter/reader at longer read distances. Preferably, the threshold voltage is approximately 800 millivolts and at least less than one volt.

The load modulators shown in FIGS. 5, 6, 10, 12 and 13 are all shown as loading a modulation impedance by switching a connection to common. However, common need not be ground but could be any available voltage reference including the low supply voltage or a voltage higher than the supply voltage. Alternatively, the load modulator loads one pad by switching a connection to the other pad. That is, rather than a connection to common, the load modulator would be connected between the pads. For example, load modulator 222 of FIG. 5 could connect to pad 232 rather than to common, as is shown in FIG. 5.

In electromagnetic RFID applications, the input capacitance measured between pads 230, 232 of integrated circuit 116 is typically not minimized, because this input capacitance is negligible after the integrated circuit is connected to an external capacitor and coil. However, in electrostatic RFID applications, where no external capacitor and coil are required, the input capacitance of the pads 230, 232 on integrated circuit 116 becomes quite important. It has been found that the input capacitance must be minimized for optimal use of integrated circuit 116 in electrostatic RFID applications. Preferably the input capacitance between pads 230, 232 is approximately 5 picofarads and at least less than approximately 10 picofarads.

For electrostatic RFID systems, it is desirable to have pads 230, 232 be as large as possible without substantially increasing the die size and parasitic capacitance. It is also desirable to have the pads spaced as far apart as the die will allow. That is, the pitch between pads is maximized.

- 5 This arrangement advantageously facilitates high volume manufacture of a tag incorporating the integrated circuit. FIG. 14 shows a plan view of a layout of a die for integrated circuit 116 allowing an optimal placement of pads 230, 232. The die has a rectangular configuration. The pads are spaced apart along the longer dimension of the die to provide maximum spacing between
10 the pads, i.e., maximum pad pitch.

- FIG. 15 shows schematically charge pump 223 and its connection to memory 220. Memory 220 is preferably an EEPROM, which requires a high voltage V_{pp} for writing to the EEPROM. Alternatively, memory 220 is preferably, ferroelectric RAM, which does not need a high programming
15 voltage. However, other types of memory are suitable for memory 220.

- Charge pump 223 generates a high voltage V_{pp} required by memory 220. Charge pump 223 has stages of capacitors that are each charged to a voltage, preferably, approximately the power supply voltage V_{cc} , then interconnected together to supply the high voltage V_{pp} required for
20 programming the EEPROM. Typically V_{pp} is around 15-18 volts.

- Charge pump 223 includes a first stage 900, a plurality of intermediate stages 902 and a final stage 904. For simplicity, in FIG. 15, two intermediate stages 902 are shown in detail with a break between the last intermediate stage shown and final stage 904. A plurality of intermediate stages 902 are
25 typically included in charge pump 223 with connections as shown between intermediate stages 902. The number of intermediate stages is determined in part by the voltage requirement for V_{pp} and by the voltage used to charge the stages.

- First stage 900 includes a capacitor C with switches 906, 908. Switch
30 906 connects a terminal 910 of capacitor C alternatively between the power supply voltage V_{cc} and a terminal 909 that serves as the high voltage V_{pp} for memory 220. Switch 908 connects a terminal 912 of capacitor C alternatively between common and a terminal 914, which is connected to a terminal 916 of the next stage of the charge pump.

- 35 Intermediate stages 902 include a capacitor C with switches 918, 920. Switch 918 connects a terminal 922 of capacitor C alternatively between power supply voltage V_{cc} and terminal 916, which is connected to the prior

stage of charge pump 223. Switch 920 connects a terminal of capacitor C alternatively between common and a terminal 924, which is connected to terminal 916 of the next stage of charge pump 223.

- 5 Final stage 904 includes a capacitor C and one switch 930. Switch 930 connects a terminal 934 of capacitor C alternatively with power supply voltage V_{cc} and terminal 932, which is connected to terminal 924 of the previous intermediate stage (not shown) of charge pump 223. Terminal 936 of capacitor C is connected to common.

- 10 Though shown as physical switches in FIG. 15, switches 906, 908, 918, 920 and 930 are preferably transistors, including bipolar and field-effect transistors connected and controlled in a manner known to those of skill in the art.

- To facilitate charging charge pump 223, switch 906 of first stage 900, switch 918 of each intermediate stage 902 and switch 930 of final stage 904 are switched to the power supply voltage V_{cc} . Also switch 908 of first stage 900 and switch 920 of each intermediate stage 902 are all switched to common and held for sufficient amount of time to allow charging of capacitors C in all the stages. Then switches 906, 908, 918, 920 and 930 are switched to their alternate positions. That is, switch 906 is connected to high voltage V_{pp} ; switch 908 is switched to terminal 914, which provides a connection to the next stage; each switch 918 is connected to terminal 916, which provides a connection to the previous stage; each switch 920 is connected to terminal 924, which provides a connection to the next stage; and switch 930 is connected to terminal 932, which provides a connection to the previous stage.

- 25 Typically, for an electromagnetic RFID application V_{cc} is approximately 2 volts or less and the high voltage V_{pp} required by the memory 220 is eighteen (18) volts. Under these circumstances, at least seven intermediate stages, a first stage and a final stage are provided for charge pump 223. In electrostatic RFID applications, the voltages coupled between the tag and exciter are substantially higher than the voltages induced in a coil in an electromagnetic application. This is explained in part due to the differences in the relationship of coupling voltage to distance in an electrostatic field versus an electromagnetic field. In an electromagnetic field the near field voltage is related to distance (D) by a function of $1/D^3$. However, the near field voltage is related to distance in an electrostatic field by a function closer to $1/D^2$ or $1/D$. This advantageously allows in electrostatic applications a higher power supply voltage V_{cc} to be readily developed or an additional voltage higher
- 35

than the power supply voltage to be readily developed. In addition, the input impedance of an electrostatic tag is much higher than the input impedance of an electromagnetic tag.

- In accordance with the invention, an integrated circuit for RFID applications is optimized for electrostatic operation by using a voltage higher than the power supply voltage to charge the stages of the charge pump. This reduces the number of stages required for the charge pump. Also, since charging the charge pump requires energy and hence power, less stages advantageously requires less power. For example, in a preferred embodiment, a voltage of 4 volts is used to charge a charge pump with 2 intermediate stages, a first stage and a final stage, to produce high voltage V_{pp} of 16 volts for programming the memory.

- Alternatively, in accordance with an alternate preferred embodiment where an integrated circuit is optimized for electrostatic operation, a high voltage V_{pp} is generated directly from the voltage coupled to the tag from the exciter, eliminating the need for a charge pump. FIG. 16 shows a block diagram of a radio frequency identification tag circuit with a memory requiring a high programming voltage V_{pp} , but this circuit does not employ a charge pump in accordance with the present invention.

- The circuit shown in FIG. 16 includes rectifier 214, high voltage regulator 1000, logic voltage regulator 1002, memory 220 and pads 230, 232. As in integrated circuit 116, rectifier 214 is coupled to pads 230, 232 to receive an electrostatic A.C. voltage that is rectified by rectifier 214 into a D.C. voltage. High voltage regulator 1000 is coupled to the D.C. voltage from the rectifier 214. High voltage regulator 1000 produces a regulated high voltage V_{pp} that is used for programming memory 220. Logic voltage regulator 1002 is also coupled to the D.C. voltage output from rectifier 214. Logic voltage regulator 1002 regulates and limits the D.C. voltage from rectifier 214 to produce a power supply voltage V_{cc} .

- Rectifier 214 is implemented in any suitable manner, including as a full-wave rectifier, a half-synchronized, full-wave rectifier or full-synchronized, full-wave rectifier or any other suitable rectifier. High voltage regulator 1000 and logic voltage regulator 1002 are implemented in any manner that provides suitable D.C. voltages, including series pass regulation or shunt regulation or any other regulation scheme. FIG. 17 is a schematic showing an embodiment of the circuit shown in FIG. 16, where rectifier 214 is shown implemented as a half-synchronized, full-wave rectifier and high voltage

regulator 1000 and logic voltage regulator 1002 are both shown implemented as shunt regulators using a zener diode to limit the output voltages.

In some applications employing radio frequency identification tags, it is desirable for the radio frequency identification tag to have a circuit state. For example, in electronic article surveillance (EAS) applications, typically, the detection of a circuit state is used to determine whether an article is authorized to be removed from a particular area. A tag with the state information receives an exciter signal and responds with a modulated signal if removal is not authorized, but does not respond with the modulated signal if removal is authorized. The circuit state, in effect, determines whether a signal is modulated or not. Radio frequency identification tags are applicable in EAS applications by maintaining a programmable circuit state as discussed in U.S. patent application serial number 09/045,357, filed 20 March 1998 by Victor Allen Vega, et al., attorney docket number IND10174, entitled "Radio Frequency Identification Tag With A Programmable Circuit State." In essence, the load modulated signal from a tag is inhibited in EAS applications based on a programmable circuit state.

FIG. 18 shows a schematic diagram of a circuit that implements a feature to defeat or inhibit load modulation based on a circuit state. The circuit includes memory 220, modulation encoder 221, controller 218, load modulator 522, gate 1004, and pads 230, 232. Memory 220 is coupled to controller 218 and modulation encoder 221 in the manner described above with respect to FIG. 3. The modulated signal output by modulation encoder 221 is received at one input of gate 1004. Controller 218 provides the other input to gate 1004. Gate 1004 is shown as an AND gate, although other logic gates and combinations of logic gates are configurable as gate 1004. The output of gate 1004 is the input signal I to load modulator 522. In accordance with the present invention, the output of controller 218, that is, the input to gate 1004, is set at a logic low level to force the input signal I to stay at a logic low level regardless of the output from modulation encoder 221. Alternatively, if the output of controller 218 is placed in a logic high state, the output from modulation encoder 221 is reflected onto the input signal I by gate 1004. Hence, the output from the controller provides a feature whereby the load modulator is enabled or disabled based on the output from the controller 218. Controller 218 retains a circuit state to determine the output used to enable or defeat the output from modulation encoder 221. In some applications, this feature is used to prevent modulation for a predetermined period of time so as

not to interfere with electronic article surveillance systems. In some embodiments, this feature is used to delay the start of modulation for a specified period of time, for example, to allow the circuit to reach a stable power-up state.

5 FIG. 19 is a block diagram showing a radio frequency identification circuit including an EAS oscillator 1006 for generating a signal for electronic — article surveillance. The circuit shown in FIG. 19 includes two load modulators 522, both capable of dampening signals on pads 230, 232. One load modulator receives the modulated signal from modulation encoder 221 in
10 the manner described with respect to FIG. 3 above. The other load modulator 522 receives a signal from a gate 1008, which receives its input from EAS oscillator 1006 and controller 218. EAS oscillator 1006 is a bit rate generator that produces a data-rate signal. In a manner similar to that described above with respect to FIG. 18, gate 1008 is controlled by controller 218 to enable or
15 disable an output from EAS oscillator 1006 from being load modulated onto pads 230, 232. This embodiment has the advantage of allowing an EAS signal to be modulated simultaneously with a normal read signal from a tag. Also, this embodiment allows the EAS signal to be defeated while still permitting the normal read tag signal to be modulated on pads 230, 232.

20 FIG. 20 shows a schematic diagram of another circuit that implements a feature to defeat or inhibit load modulation based on a circuit state. The circuit includes memory 220, modulation encoder 221, controller 218, transmit modulator 222', gate 1004, and pad 303. Memory 220 is coupled to controller 218 and modulation encoder 221 in the manner described above with respect
25 to FIG. 4. The modulated signal output by modulation encoder 221 is received at one input of gate 1004. Controller 218 provides the other input to gate 1004. Gate 1004 is shown as an AND gate, although other logic gates and combinations of logic gates are configurable as gate 1004. The output of gate 1004 is the input signal I to transmit modulator 222'. In accordance with
30 the present invention, the output of controller 218, that is, the input to gate 1004, is set at a logic low level to force the input signal I to stay at a logic low level regardless of the output from modulation encoder 221. Alternatively, if the output of controller 218 is placed in a logic high state, the output from modulation encoder 221 is reflected onto the input signal I by gate 1004.
35 Hence, the output from the controller provides a feature whereby the transmit modulator 222' is enabled or disabled based on the output from the controller 218. Controller 218 retains a circuit state to determine the output used to

- enable or defeat the output from modulation encoder 221. In some applications, this feature is used to prevent modulation for a predetermined period of time so as not to interfere with electronic article surveillance systems. In some embodiments, this feature is used to delay the start of modulation for a specified period of time, for example, to allow the circuit to reach a stable power-up state.
- 5

- The present invention provides an optimized method and circuit for electrostatic radio frequency identification tags. More specifically, a modulation circuit in accordance with the invention includes improved impedance and threshold voltage characteristics that improve efficiency and read ranges. Also charge pump stages are reduced or eliminated in accordance with the invention. This substantially reduces current consumption. These improvements advantageously allow better performance and better efficiency over prior electromagnetic radio frequency identification tags.
- 10
- 15

While the present invention optimizes, in particular, electrostatic radio frequency identification tags, the improved radio frequency identification circuit is still useful for electromagnetic radio frequency identification tags.

- Whereas the present invention has been described with respect to specific embodiments thereof, it will be understood that various changes and modifications will be suggested to one skilled in the art and it is intended that the invention encompass such changes and modifications as fall within the scope of the appended claims.
- 20

What is claimed is:

Claims

- 5 1. A radio frequency identification tag comprising:
 a first antenna element;
 a second antenna element electrically isolated from the first antenna
 element; and
 a radio frequency identification circuit having a first pad and a second
10 pad, said first and second pads being coupled, respectively, to said first and
 second antenna elements, said radio frequency identification circuit including
 a load modulation circuit coupled to at least one of said first and second pads
 that produces an amplitude modulated signal on said at least one of said first
 and second pads, wherein said amplitude modulated signal varies from a first
15 amplitude to a second amplitude different from the first amplitude, said
 second amplitude being determined in part by a modulation impedance.
2. The tag of claim 1 wherein said load modulation circuit comprises a
 modulation switch and said modulation impedance is connected in series with
20 said at least one of said first and second pads and said modulation switch
 and said modulation switch is connected to a voltage reference.
3. The tag of claim 2 wherein said modulation impedance comprises at
 least one of a resistor;
25 a capacitor;
 a resistor connected to a capacitor; and
30 a field-effect transistor.
4. The tag of claim 3 wherein said resistor is at least 100 ohms.
5. The tag of claim 2 wherein said modulation switch comprises at least
35 one of a bipolar transistor; and

6. The tag of claim 2 wherein said modulation switch comprises a plurality of bipolar transistors connected in a Darlington configuration.

- 40 7. A radio frequency identification tag comprising:
a first antenna element;
a second antenna element electrically isolated from the first antenna element;
a radio frequency identification circuit having a first pad and a
45 second pad, said first pad being coupled to said first antenna element and said second pad being coupled to said second antenna element; and
wherein said radio frequency identification circuit includes a load modulation circuit coupled to said first pad and said second pad to selectively dampen a modulated signal on said first pad and another modulated signal
50 on said second pad in response to an input signal received by said load modulation circuit.

8. A radio frequency identification tag comprising:
a first antenna element;
55 a second antenna element electrically isolated from the first antenna element; and
a radio frequency identification circuit having a first pad and a second pad, said first and second pads being coupled, respectively, to said first and second antenna elements, said radio frequency identification circuit including
60 a load modulation circuit coupled to at least one of said first and second pads that produces a modulated signal that varies from a first amplitude to a second amplitude in response to a signal that must exceed a predetermined voltage threshold before said modulation circuit produces said modulated signal.

- 65 9. The tag of claim 8 wherein said predetermined threshold voltage is below one volt.

- 70 10. A radio frequency identification tag comprising:
a first antenna element;
a second antenna element electrically isolated from the first antenna element; and

75 a radio frequency identification circuit having a first pad and a second pad, said first and second pads being coupled, respectively, to said first and second antenna elements, said first pad and said second pad having an capacitance as measured between said first and second pads.

80 11. The tag of claim 10 wherein the input capacitance is less than 10 picofarads.

12. A method of optimizing a radio frequency identification tag comprising the steps of:

85 A) providing a first antenna element;

B) providing a second antenna element that is electrically isolated from the first antenna element;

C) providing a radio frequency identification circuit having a first pad and a second pad, said radio frequency identification circuit including a load modulation circuit coupled to at least one of said first and second pads, said load modulation circuit producing an amplitude modulated signal that varies from a first amplitude to a second amplitude in response to an input signal that exceeds a predetermined threshold voltage before said modulation circuit produces a modulated signal; and

90 D) coupling said first antenna element to said first pad and said second antenna element to said second pad.

100 13. The method of claim 12 wherein the threshold voltage is in the range of 0.8 to 1 volt.

14. A radio frequency identification tag comprising:

a first antenna element;

105 a second antenna element electrically isolated from the first antenna element;

a radio frequency identification circuit having a first pad and a second pad, said first and second pads being coupled, respectively, to said first and second antenna elements;

110 wherein said radio frequency identification circuit includes a memory
that requires a high voltage for programming said memory, the high voltage
being higher than a nominal supply voltage; and

wherein the high voltage is supplied by a charge pump, said charge
pump including a plurality of capacitors.

115

15. A radio frequency identification tag comprising:

a first antenna element;

a second antenna element electrically isolated from the first antenna
element;

120 a radio frequency identification circuit having a first pad and a second
pad, said first and second pads being coupled, respectively, to said first and
second antenna elements;

wherein said radio frequency identification circuit includes a memory
that requires a high voltage for programming said memory, the high voltage
125 being higher than a nominal supply voltage; and

wherein the high voltage is supplied by a circuit comprising:

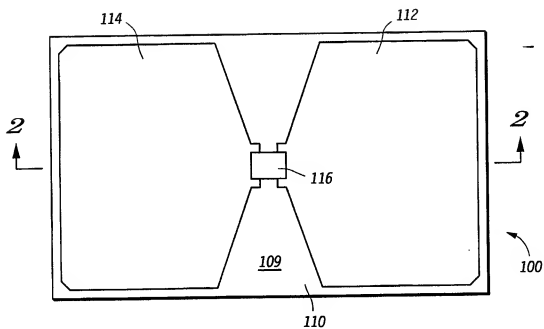
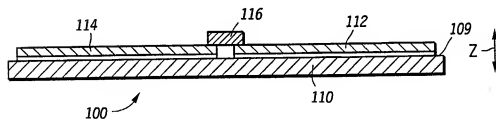
a rectifier that rectifies an A.C. voltage from said antenna
elements to produce a rectified voltage; and

130 a high voltage regulator that receives the rectified voltage and
produces the high voltage for said memory.

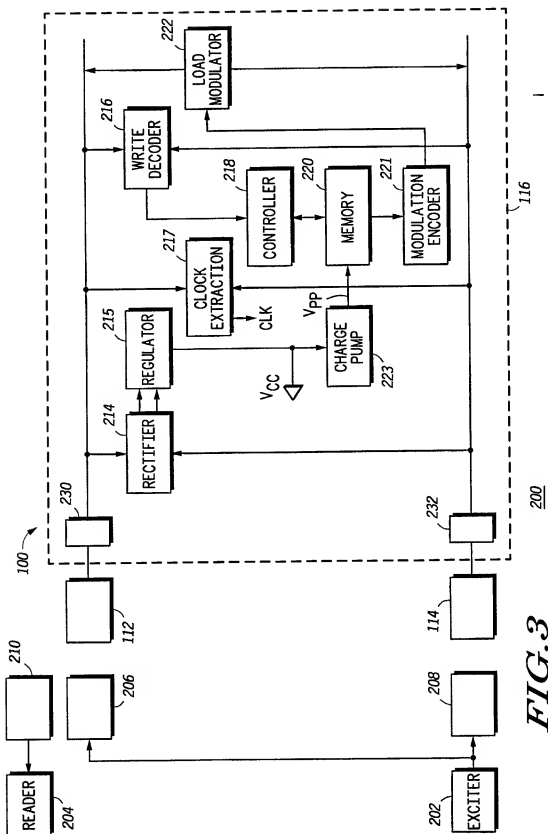
16. The tag of claim 15 wherein said circuit state changes at a
predetermined time after the radio frequency identification circuit receives
power.

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1/13

*FIG. 1**FIG. 2*

2/13



3/13

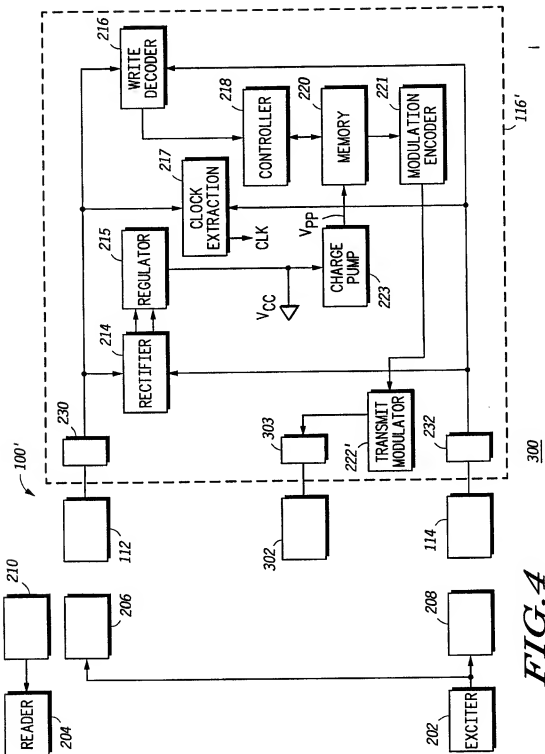
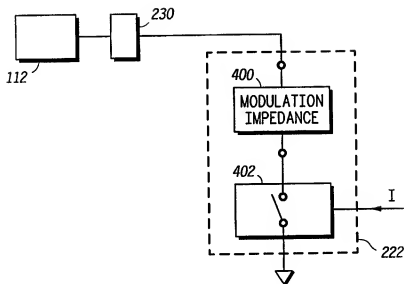
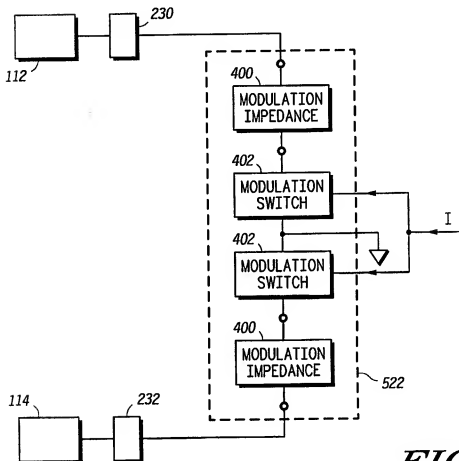
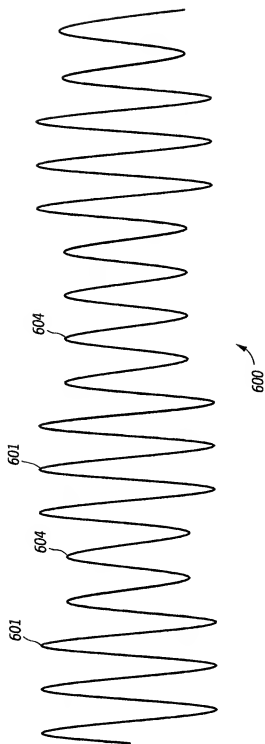


FIG. 4

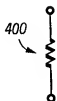
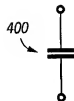
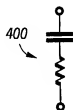
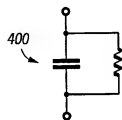
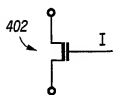
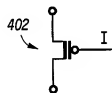
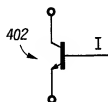
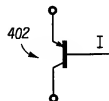
4/13

*FIG. 5**FIG. 6*

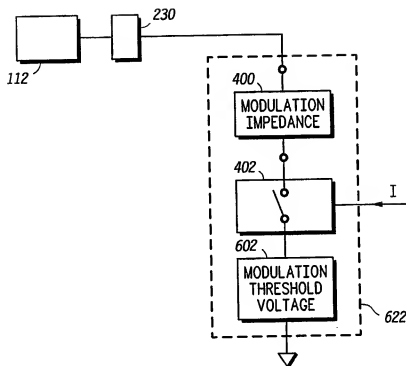
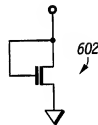
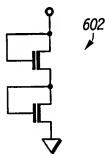
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**FIG. 7**

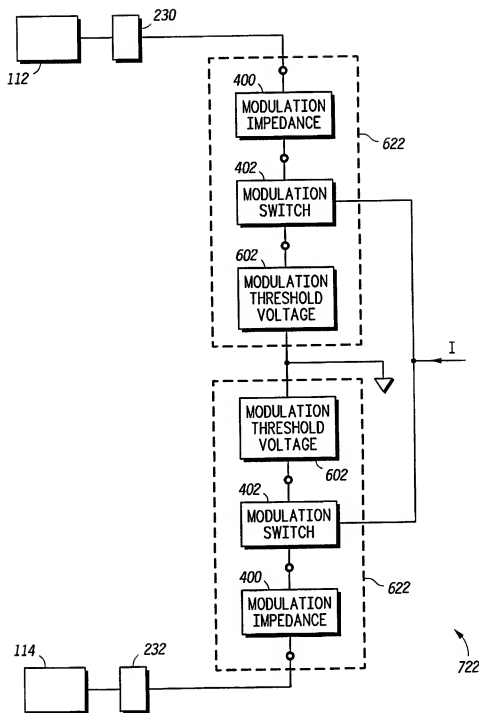
6/13

*FIG. 8A**FIG. 8B**FIG. 8C**FIG. 8D**FIG. 9A**FIG. 9B**FIG. 9C**FIG. 9D*

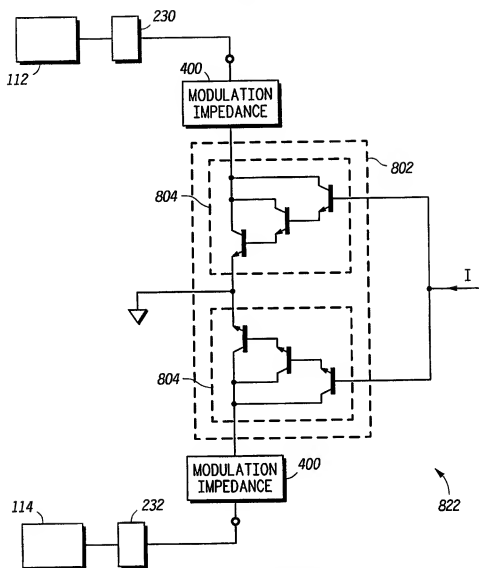
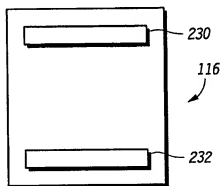
7/13

*FIG. 10**FIG. 11A**FIG. 11B**FIG. 11C*

8/13

**FIG. 12**

9/13

**FIG. 13****FIG. 14**

10/13

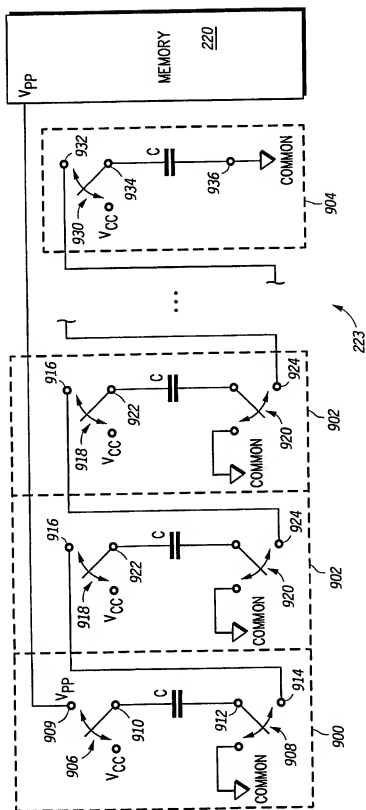
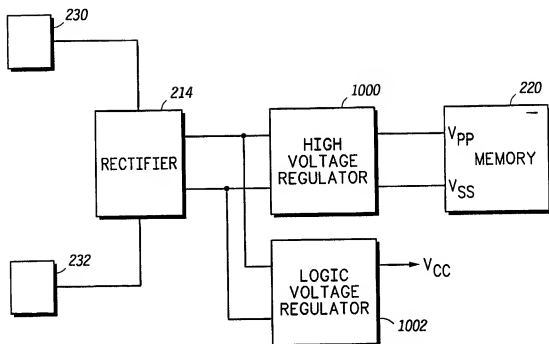
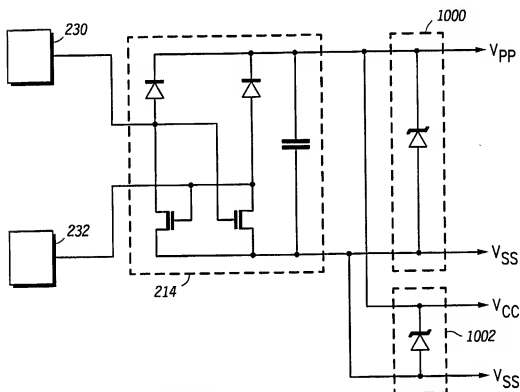


FIG. 15

11/13

**FIG. 16****FIG. 17**

12/13

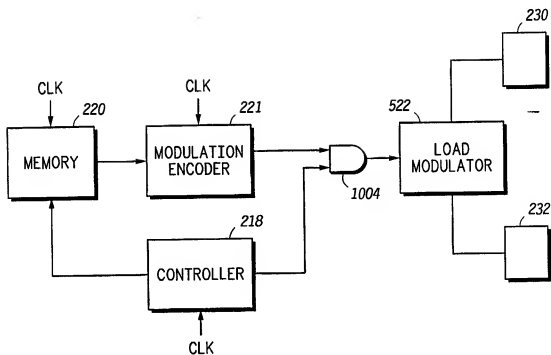


FIG. 18

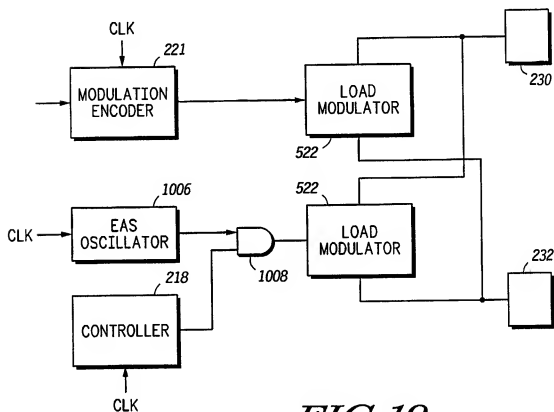
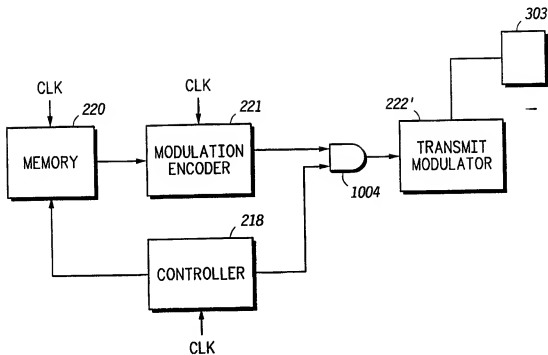


FIG. 19

13/13

*FIG. 20*

INTERNATIONAL SEARCH REPORT

 International application No.
 PCT/US99/20307

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :G04B 13/14

US CL :340/572.7, 825.34, 825.54

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 340/572.7, 825.34, 825.54, 572.1; 342/44, 51; 257/679

 Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
 NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS (pad, antenna, IC, identification, RFID, terminal)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5,099,227 A (GEISZLER et al) 24 March 1992.	1-16
A	US 5,682,143 A (BRADY et al) 28 October 1997.	1-16

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:	*T	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
A document defining the general state of the art which is not considered to be of particular relevance	*X*	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
B earlier document published on or after the international filing date	*Y*	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
L document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	*A*	document member of the same patent family
O document referring to an oral disclosure, use, exhibition or other means		
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 Date of the actual completion of the international search
 12 OCTOBER 1999

Date of mailing of the international search report

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